REMARKS

Claims 1-24 are pending in this application. In the January 13, 2004, Office Action, claims 1, 3-5, 8, 10, 11, 14-17, 19, 21 and 22 were rejected as anticipated by a patent to Jones (US No. 6,590,901). Claims 2, 12, 13 and 20 were deemed to be obvious in view of Jones, while claim 6 was indicated to be obvious in view of the combination of Jones with US Patent No. 6,137,807 to Rusu.

Applicants appreciate the indication of allowable subject matter in pending claims 7, 9, 18, 23 and 24. For the reasons noted herein, Applicants have not made these claims independent as suggested in the Office Action because it is believed that certain intervening claims are patentable over the art of record.

Applicants have amended claim 2 to place it in independent form by incorporating the limitations from its base claim 1. Claim 3 was amended to change its dependency to claim 2. Claim 10 was amended to correct its dependency to claim 9. Claims 6 and 7 were amended to correctly identify the plurality of logical memory devices.

Applicants have also amended claim 12 to place it in independent form by incorporating the limitations of its base claim 11. Claims 13-15 have been amended to change their dependency to claim 12. Claim 18 was amended to correct a grammatical error. Claim 13 has been amended to recite fourth and fifth memory devices in light of its dependency on amended claim 12, which defines three logical memory devices.

Finally, claim 20 has been amended to place it in independent condition by incorporating the limitations of its base claim 19. Claims 21- 23 have been amended to change their dependency to claim 20, and claim 24 to depend from claim 23. None of the present amendments to claims 2, 3, 6, 7, 10, 12-15, 18, and 20-24 were made for substantive reasons in light of the prior art rejections in this Office Action.

Independent claims 2, 12 and 20 share a common point of novelty over the art of record, namely the structure and method steps for writing a third portion of a data packet to a third logical memory device. None of the art of record discloses or suggests segmenting an incoming data packet into three portions, each of which is stored in three different logical memory devices. In one embodiment of the present invention, a first portion of a data packet is stored in memory module 660, as described at page 15, lines 3-16, of the specification. The

remaining data of the packet is written in distinct burst write segments to one of the modules 630(a)-(f). In a specific example, the first 8 bits of data is written to module 660, while 32 bit bursts are written to the second and third memory modules from the modules 630. This additional memory module 660 is used to store packet data as well as address lookup information, as explained at page 12, lines 7-13 of the specification. This data is accessed by the ARL to map received data packets to an outgoing port, as described at pages 24-27 of the specification.

Contrary to the assertion in the Office Action, Jones does not contemplate the memory management approach defined in Applicants' claims. In rejecting claims 2, 12 and 20 as obvious, it was suggested that a person of skill would have been motivated to add more PBRAMs to increase the memory capacity of the memory array 62 of Jones. However, these claims of the present application concern more than simply adding memory modules. These claims also define parsing a data packet into three portions and storing these portions in separately accessible memory modules. This memory management approach improves access times and makes more efficient use of a limited memory. Thus, rather than add additional memory modules, as suggested in the Office Action, the present invention provides a novel memory management approach, as defined in claims 2, 12 and 20. Moreover, storage of incoming data packet in three portions enhances the ability of the present inventive network switch to transmit the data packets to their requested destination.

There is nothing in Jones or any of the other references of record that disclose or suggest separating an incoming data packet into three portions, as set forth in Applicants' claims 2, 12 and 20. At best, Jones discloses separating an incoming packet into two portions for storage in two PBRAMs, as depicted in FIG. 11 and discussed at col. 11, lines 31-51. As explained in this excerpt, Jones simply contemplates an alternate storage scheme in which all packets are distributed evenly across all PBRAMs so that all the PBRAMs can operate in lock-step without any communication between them. This discussion in Jones falls short of providing the motivation for the three portion – three logical memory device approach defined in Applicants' claims.

It is therefore believed that claims 2, 12 and 20 are patentable over the art of record. Since all of the remaining claims depend from these claims, they too are believed to be

patentable. It can be noted that claims 7, 9, 18, 23 and 24 have already been deemed to contain allowable subject matter, and this conclusion is not altered by their dependency on newly independent claims 2, 12 and 20.

For all of the foregoing reasons, it is respectfully submitted that Applicants have made a patentable contribution to the art. Favorable reconsideration and allowance of this application is, therefore, respectfully requested.

Respectfully submitted,

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